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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,036	12/03/2003	Cam L. Lu	03-1978 81641	9432

7590 08/16/2005

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EXAMINER


SIEK, VUTHE

ART UNIT PAPER NUMBER

2825

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/728,036	Applicant(s) LU ET AL. 	
	Examiner Vuthe Siek	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address.--

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 December 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/3/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to application 10/728,036 filed on 12/3/2003.

Claims 1-16 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-16 are rejected under 35 U.S.C. 102(a) as being anticipated by Lin et al., "High-Frequency, At-Speed Scan Testing," IEEE, October 2003, pp. 17-25.

4. As to claims 1 and 9, Lin et al. teach substantially similar claimed invention of a method of generating a truncated scan test pattern for an integrated circuit (IC) design (see entire document) comprising a) receiving as input an IC design; b) estimating a number of transition delay fault test patterns and a corresponding number of top-off stuck-at fault patterns to achieve maximum stuck-at fault and transition delay fault coverage; c) truncating the estimated number of transition delay patterns to generate a truncated set of transition delay fault patterns so that the truncated set of transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns achieve maximum stuck-at fault and transition delay fault coverage within a selected scan memory limit; and d) generating as output the truncated set of transition delay

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fault patterns and the corresponding number of top-off stuck-at fault patterns (especially see pages 21-24).

5. As to claims 2-8 and 10-16, Lin et al. teach wherein step (b) comprises generating a set of stuck-at fault test patterns (at least page 21); ordering the set of stuck-at fault patterns according to fault coverage to generate a set of ordered stuck-at fault patterns; generating a plot of fault coverage as a function of a number of stuck-at fault patterns from the ordered set of stuck-at fault patterns (at least page 21); generating a set of transition delay fault patterns for each scan clock domain in the integrated circuit design (Fig. 5-6); ordering the transition delay fault patterns in the set of transition delay fault patterns for each scan clock domain according to stuck-at fault coverage to generate an ordered set of transition delay fault patterns for each scan clock domain (pages 21-24); ordering each ordered set of transition delay fault patterns according to a number of transition delay fault patterns therein to generate the estimated number of transition delay fault patterns (pages 21-24); generating a plot of transition delay fault coverage as a function of a number of transition delay fault patterns from the total set of transition delay fault patterns (pages 21-24).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek


**VUTHE SIEK
PRIMARY EXAMINER**